22. (New) A communication circuit comprising:

an amplifier comprising a capacitor to provide compensation, the capacitor comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a base, emitter, and collector;

wherein bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the base and collector of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

Remarks

Claims 1, 9-17, and 21-22 are presently active, claims 2-8 and 18-20 having been cancelled without prejudice by this Amendment, and new claims 21 and 22 added by this Amendment.

An informality is corrected in the specification.

In the office action dated 15 February 2002 ("Office Action"), claims 17-20 were rejected under 35 U.S.C. §112, second paragraph; claims 9, 10, and 13 were rejected under 35 U.S.C. §102(e) as being anticipated by Williamson, U.S. patent 6,194,973B1 ("Williamson"); claims 1-5 and 8-10 were rejected under 35 U.S.C. §102(b) as being anticipated by Hariton, U.S. patent 5,926,064 ("Hariton"); claims 6, 7, 11, and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hariton; and claims 13-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art Fig. 2 and in view of Hariton.

35 U.S.C. §112, second paragraph rejection of claims 17-20

In the Office Action, page 2, item no. 3, it was stated that claims 17-20 had omitted elements because the amplifier merely comprised a capacitor.

Applicant respectfully traverses this rejection. As stated in the Office Action, for an amplifier to amplify, it must comprise much more than merely a capacitor. But there is no legal requirement that a claim must contain necessary elements for the claimed invention to work. To satisfy 35 U.S.C. §112, second paragraph, it is only necessary for the claim to particularly point out and distinctly claim the subject matter of the invention. That is, can one reading the claims determine whether or not the claims read upon his or hers device?

It is believed that claim 17 satisfies 35 U.S.C. §112, second paragraph. One reading the claim may readily determine if they have an infringing device. Claim 17 would read on any amplifier using a capacitor for compensation, where the capacitor comprises the first and second field effect transistors, and the bias transistor, as recited in the claim. It is not necessary to further narrow the claim to a particular type of amplifier by including elements essential to a working model, such as, for example, current sources, differential input stages, current mirrors, etc.

Consequently, Applicant believes that all presently active claims satisfy 35 U.S.C. §112, second paragraph.

35 U.S.C. §102(e) rejection of claims 9, 10, and 13 in view of Williamson

In the Office Action, page 2, item no. 4, reference was made to transistors MCX0 and MCX1, and transistor M2 in Williamson, Fig. 9.

Applicant does not believe that Williamson anticipates the claims as now amended. Referring to Fig. 9, transistor M2 does not have its gate connected to its drain. As can be seen from Fig. 9, the gate of M2 is connected to V_{SS} (substrate or ground), but the drain of M2 is connected to the terminal X0, which is also connected to the drain of transistor M1.

However, claims 9, 10, and 13 recite that the gate and drain of the bias transistor are connected to each other. Consequently, claims 9, 10, and 13 are not anticipated by Williamson.

35 U.S.C. §102(b) rejection of claims 1-5 and 8-10 in view of Hariton

Claim 1 is amended to include the limitations of claims 3-5, which have been cancelled without prejudice. Consequently, no new matter has been added to amended claim 1. Claim 8 has also been cancelled, so that the claims at issue under this rejection are claims 1, 9, and 10.

Applicant respectfully traverses the 35 U.S.C. §102(b) rejection of claims 1, 9, and 10, for the following reasons.

In the Office Action, page 3, item no. 5, reference was made to Fig. 5 of Hariton. Specifically, reference was made to FET 505 of Fig. 5 in Hariton. Note that FET 505 is biased by transistor 504 to have a source-drain current of I_{REF}. However, claim 1 recites that the bias transistor has a substantially zero DC bias current. Consequently, FET 505 cannot be identified with the bias transistor claimed in claim 1.

Claim 9, and claim 10 by virtue of its dependency upon claim 9, recite that the drain and gate of the third field effect transistor are connected to each other and to the sources and drains of the first and second field effect transistors. Note that the gate and drain of FET 505 are not connected to the sources and drains of transistors 302 and 303. Consequently, FET 505 cannot be identified with the third field effect transistor claimed in claims 9 and 13.

Furthermore, although not discussed in the Office Action, Applicant remarks that FET 504 cannot be identified with the bias transistor as recited in claim 1. Note that the gate of FET 504 is biased by FET 505. Either the drain of FET 504 is the same voltage potential as its gate, or it is not. If the drain of FET 504 were to be fixed at the voltage potential of its gate, then it would mirror the current I_{REF}. But claim 1 recites that the bias transistor has substantially zero DC bias current, and consequently FET 504 cannot be identified with the bias transistor. On the other hand, if the drain of FET 504 were not fixed at the voltage potential of its gate, then it immediately follows that FET 504 cannot be identified with the bias transistor of claim 1 because claim 1 recites that the gate and

drain of the bias transistor are substantially at the same voltage potential. Therefore, FET 504 cannot be identified with the bias transistor of claim 1.

Furthermore, FET 504 cannot be identified with the third field effect transistor as recited in claims 9 and 10, because these claims explicitly recite that the third field effect transistor has its gate and drain connected to the sources and drains of the first and second field effect transistors, and this is not the case with FET 504.

Consequently, Applicant believes that claims 1, 9, and 10 are not anticipated by Hariton.

35 U.S.C. §103(a) rejection of claims 6, 7, 11, and 12 in view of Hariton

This rejection is based upon the 35 U.S.C. §102(b) rejection of claims 1-5 and 8-10 and the argument that it is well known to use bipolar junction transistors instead of field effect transistors for current mirrors or biasing. (See Office Action, page 3, item no. 7.) However, for the same reasons as given above regarding the 35 U.S.C. §102(b) rejection of claims 1-5 and 8-10 in view of Hariton, Applicant traverses this rejection.

35 U.S.C. §103(a) rejection of claims 13-20 in view of Applicant's Fig. 2 and Hariton

Fig. 2 of the present application is cited only because it teaches a communication device with an amplifier having a capacitor connected as shown. (See Office Action, page 4, item no. 8.) However, for the same reasons as given above regarding the 35 U.S.C. §102(b) rejection of claims 1-5 and 8-10 in view of Hariton, Applicant traverses this rejection.

Respectfully submitted,

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Version of Amended Specification and Claims Showing Changes

In the Specification

In many applications, there is a need for a high density capacitor using a digital CMOS (Complementary Metal Oxide Semiconductor) process in which the voltage difference between the terminals of the capacitor [are] is small. For example, Fig. 2 illustrates operational amplifier (OPAMP) **202**, which is part of some larger circuit **222**, such as, for example, an analog-to-digital converter, or a communication circuit such as an Ethernet PHY. OPAMP **202** comprises first differential stage **204** and a final output stage comprising nMOSFET **206** biased by current source **210**, where the output signal is taken at output port **212** and input signals are applied at input ports **214** and **216**. Miller compensation is applied to nMOSFET **206** by connecting capacitor **208** as shown in Fig. 2. Other stages, employing nMOSFETs, pMOSFETs, or both types of transistors, may be present in OPAMP **202**, but for simplicity are not shown. The voltage difference between terminals **218** and **220** of capacitor **208** may be small, such as much less than 0.1 volts.

In the Claims

1. (Amended) A device comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a gate, source, and drain;

wherein bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the gate and drain of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

[a bias transistor, wherein the sources and drains of the first and second field effect transistors are coupled to the bias transistor so that an impedance between the gates of the first and second field effect transistors is substantially capacitive.]

17. (Amended) A communication circuit comprising:

an amplifier comprising a capacitor to provide compensation, the capacitor comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a gate, source, and drain;

wherein bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the gate and drain of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

[a bias transistor, wherein the sources and drains of the first and second field effect transistors are coupled to the bias transistor so that an impedance between the gates of the first and second field effect transistors provides the compensation.]